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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,170	11/14/2001	Eugene P. Matter	42390P12396	7336

8791 7590 03/24/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
MCLEAN-MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,170	MATTER ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on November 14, 2001.

Specification

2. The disclosure is objected to because of the following informalities:

The title of the Application is misspelled, "Memory Adaptedt to Provide Dedicated and/or Shared Memory to Multiple Processors and Method Therefor".

Adaptedt is spelled incorrectly. Appropriate correction is required.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 11 is objected to because of the following informalities:

Claim 11, line 3 states "coupled". This should state "couple".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 33 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 33 recites the limitation "the second portion" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 3-13, 15, 17-21, 30 and 33-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Cherabuddi (PGPUB: US 2002/0184445).

Regarding claims 1, 3-4, 9-10, 17 and 21, Cherabuddi discloses an apparatus comprising a memory array (Figure 2, Reference 23) having a first portion (Figure 2, Reference 23a) and a second portion (Figure 2, Reference 23b), the first portion of the memory array being different than the second portion of the memory array (page 2; section [0019]; lines 6-9), wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor (Figure 2, Reference 21a) and the second portion of the memory array is

accessible only by a second processor (Figure 2, Reference 21b) (page 2; section [0023], lines 11-19).

Regarding claims 5-6, Cherabuddi discloses dynamically altering a size of the first portion and the second portion of the memory array depending on an operational load (indicated by the active state of the processor) of the first and second processor (pages 2-3; section [0025] – when the system operates in state 1T, the first portion size is doubled and the second portion size is zero).

Regarding claims 7-8, Cherabuddi discloses the first processor accessing the first portion of the memory array substantially simultaneously as the second processor access the second portion of the memory array (pages 3-4; section [0034]; - the first and second processor are granted exclusive access simultaneously to the first and second amount of memory and thus the first processor may read to the first portion of memory simultaneous with the second processor writing to the second portion of memory).

Regarding claims 11-12 Cherabuddi discloses a first bus to couple the first processor to the first portion of the memory array and a second bus to couple the second processor to the second portion of the memory array (refer to Figure 2).

Regarding claim 13, Cherabuddi discloses a bus to couple the first and second processor to the memory array (Figure 2 - comprised of the signal lines coupling References 21a-21b to 23).

Regarding claim 15, Cherabuddi discloses a memory controller coupled to the first processor and the second processor (Figure 2, Reference 22); and a bus to couple the memory controller to the memory array (Figure 2 – signal lines coupled to Reference 23 and 22).

Regarding claims 18-19, Cherabuddi discloses dynamically altering a size of the first portion and the second portion of the memory depending on an operational load (indicated by active state of the processor) of the first processor or the second processor (pages 2-3; section [0025] – when the system operates in state 1T, the first portion size is doubled and the second portion size is zero).

Regarding claim 20, Cherabuddi discloses the first and second processor accessing the first and second portion of memory respectively substantially simultaneously (pages 3-4; section [0034]).

Regarding claim 30, Cherabuddi discloses increasing a first amount of a memory array that is accessible only by a first processor while reducing a second amount of memory array that is accessible only by a second processor (page pages 2-3; section [0025] – when the system operates in state 1T, the first portion size is doubled and the second portion size is zero).

Regarding claims 33-34, Cherabuddi discloses writing (accessing) to the first amount of the memory array substantially simultaneous with reading (accessing) the second portion of the memory with the second processor (pages 3-4; section [0034]; - the first and second processor

are granted exclusive access simultaneously to the first and second amount of memory and thus the first processor may write to the first amount of memory simultaneous with the second processor reading the second amount of memory).

10. Claim 22 and 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Kermani (USPN: 6,314,499).

Kermani discloses a first processor (Figure 2, Reference 100; C 3, L 45-48); a second processor (Figure 2, Reference 104; C 3, L 45-48); a memory bus (Figure 2; C 3, L 54-62); a memory array (Figure 2, Reference 200a), wherein the first processor and the second processor are coupled to the memory array by the memory bus (C 3, L 54-62; C 4, L 55-58); and an arbitrator to resolve access conflicts to the memory array by the first and second processor (C 4, L 23-58).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 14 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi (PGPUB: US 2002/0184445) in view of Tarui (USPN: 6,088,770).

Cherabuddi discloses the limitations cited above, however, Cherabuddi does not disclose a collision detector to arbitrate access to the first portion and the second portion of the memory array by the first and second processor. However, Tarui teaches the concept of arbitrating access

to a first memory portion and second memory portion to prevent a processor from accessing memory not allocated to it (C 12, L 31-67; C 13, L 1-5). This feature taught by Tarui ensures proper functioning of the system by allowing a processor to only access memory portions allocated to it, thereby ensuring accuracy of the data. Cherabuddi does not disclose any measures for ensuring that a processor only accesses a memory portion allocated to it and thus Cherabuddi's system is vulnerable to data inaccuracies. Hence, it would have been obvious to one of ordinary skill in the to use Tarui's teachings with the teachings of Cherabuddi for the desirable purpose of data accuracy.

13. Claims 2, 16 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherabuddi (PGPUB: US 2002/0184445) in view of Kirk (USPN: 5,875,464).
Cherabuddi discloses the limitations cited above, however, Cherabuddi does not disclose a third portion of memory different than the first and second portion of memory, wherein the third portion of the memory array is accessible by the first processor and the second processor. Kirk teaches the concept of private and shared memory partition (Figure 4; C 13, L 26-67; C 14, L 1-4). This feature taught by Kirk allows data sharing in the shared partition and allows non-data sharing in the private partition, which provides flexibility. In Cherabuddi, the partitions are dedicated and do not allow for data sharing. Hence, it would have been obvious to one of ordinary skill in the art to use Kirk's teachings with the system taught by Cherabuddi for the desirable purpose of flexibility.

14. Claims 23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani (USPN: 6,314,499) in view of Cherabuddi (PGPUB: US 2002/0184445). Kermani discloses the limitations cited above in claim 22, however, Kermani does not disclose the memory array comprising a first portion and a second portion, wherein the first portion is accessible only by the first processor and the second processor is accessible only by the second processor, wherein the first processor is permitted to access (read or write) the first portion of the memory array as the second processor accesses (read or write) the second portion of the memory array. However, Cherabuddi discloses a memory array (Figure 2, Reference 23) having a first portion (Figure 2, Reference 23a) and a second portion (Figure 2, Reference 23b)(page 2; section [0019]; lines 6-9), wherein the first portion of the memory array is accessible only by a first processor (Figure 2, Reference 21a) and the second portion of the memory array is accessible only by a second processor (Figure 2, Reference 21b) (page 2; section [0023], lines 11-19). This features taught by Cherabuddi improves the performance of the system by allowing each processor to access a portion of the memory exclusively thereby reducing latency by preventing a processor from having to wait to access memory because another processor is accessing the memory. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Cherabuddi's teachings with the system taught by Kermani for the desirable purpose of improved performance.

15. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani (USPN: 6,314,499) in view of Cherabuddi (PGPUB: US 2002/0184445) as applied to claim 23 and further in view of Kirk (USPN: 5,875,464).

Kermani and Cherabuddi disclose the limitations cited above in claim 23, however, Kermani and Cherabuddi do not disclose the memory array comprising a third portion that is accessible by both the first processor and the second processor. However, Kirk teaches the concept of private and shared memory partition (Figure 4; C 13, L 26-67; C 14, L 1-4). This feature taught by Kirk allows data sharing in the shared partition and allows non-data sharing in the private partition, which provides flexibility. In the system taught by Kermani and Cherabuddi, the partitions are dedicated and do not allow for data sharing. Hence, it would have been obvious to one of ordinary skill in the art to use Kirk's teachings with the system taught by Kermani and Cherabuddi for the desirable purpose of flexibility.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu – USPN: 5,659,715 – dynamic memory allocation.

Noel – PGPUB: US 2002/0016891 – shared memory system.

Luan – USPN: 5,911,149 – shared memory system and memory allocation.

Zalewski – PGPUB: US 2002/0052914 – shared memory system.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

March 19, 2003